Abstracts

Parasitic-aware design and optimization of CMOS RF integrated circuits (1998 [RFIC])

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The need for higher integration and lower cost personal communication systems (PCS) has motivated extensive efforts to develop CMOS RF integrated circuits which meet the performance requirements of current and future standards such as IS-95, GSM, DECT, etc. However, power losses associated with on-chip inductor, device, and package parasitics have impeded the full integration of power-efficient CMOS RF ICs. In this paper, we describe a custom CAD synthesis and optimization tool which enables RF chip/package design for optimum circuit performance. A fully-integrated CMOS power amplifier (PA) illustrates the efficacy of this approach.

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